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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: **GARNIER ET AL.**	
Serial No. **09/499,060**	Examiner: **T. Cunningham**
Confirmation No. **9699**	Art Unit: **2816**
Filing Date: **February 4, 2000**	
For: **VOLTAGE RAMP GENERATOR AND CURRENT RAMP GENERATOR INCLUDING SUCH A GENERATOR**	

APPELLANTS' APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellants' Appeal Brief. The requisite $320.00 large entity fee for filing the brief was initially paid on May 20, 2003 when this brief was initially filed. However, the Examiner reopened prosecution. The requisite $320.00 large entity fee initially paid is now being applied to the present brief. If any additional fee is required, authorization is given to charge Deposit Account No. **01-0484**.

(1) Real Party in Interest

The real party in interest is STMicroelectronics S.A., a French corporation.

(2) Related Appeals and Interferences

At present there are no related appeals or interferences.

In re Patent Application of:
GARNIER ET AL.
Serial No. **09/499,060**
Filing Date: **February 4, 2000**

(3) Status of the Claims

The rejection of Claims 9-37 and 40 is being appealed. These claims are listed in the attached Appendix (9). Claims 38 and 39 have been cancelled.

(4) Status of Amendments

All amendments have been entered and there are no further pending amendments.

(5) Summary of the Invention

The present invention is directed to an integrated circuit voltage ramp generator produced using CMOS technology. The integrated circuit voltage ramp generator comprises a capacitance **C** and a CMOS charging circuit **Ig2, T4, T5, Re** connected to the capacitance, as best shown in FIG. 3 from the original specification and reproduced below for convenience, and as described on pages 5-9 of the application.

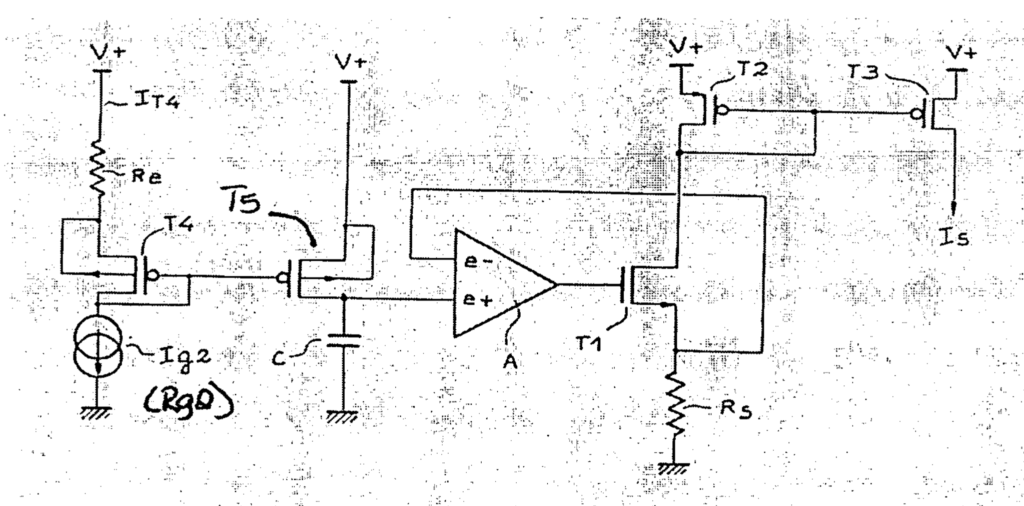

FIG. 3 from the Appellants' specification

The CMOS charging circuit comprises a current generator **Ig2** having a first resistance **Rg2**, and a circuit **T4, T5** connected to the current generator and to the capacitance **C**. The circuit **T4, T5** also has a second resistance **Re** which enables a capacitance charging current to be proportional to a square of a ratio of the second resistance **Re** and the first resistance **Rg2**.

Since the first and second resistances **Rg2, Re** are formed using CMOS technology, their respective spreads can be more easily compensated. This spread may be due to operating temperature changes, for example. As discussed on page 7, lines 11-24 of the Appellants' specification, the second resistance **Re** may be chosen with a temperature variation coefficient of the same order of magnitude as that for the first resistance **Rg2**, for example. This advantageously allows compensation for variations in temperature due to the first resistance **Rg2**.

Without the second resistance **Re**, the spread of the first resistance **Rg2** may be reflected in variations of the capacitance charging current. To compensate for the spread of the first resistance **Rg2**, the second resistance **Re** is included. The capacitance charging current is thus controlled based upon the ratio of the second and first resistances **Re** and **Rg2**. In particular, the capacitance charging current is proportional to a square of a ratio of the second resistance **Re** and the first resistance **Rg2**.

(6) Issues

The issue presented on appeal is whether Claims 9-37 and 40 is unpatentable under 35 U.S.C. §103 over the Appellants' prior art FIG. 1 in view of the Tanigawa patent (U.S. Patent No. 4,814,724) and in view of the Lauffenburger patent (U.S. Patent No. 5,254,957).

(7) Grouping of Claims

Claims 9-37 and 40 stand or fall together.

(8) Arguments

I. The Claims

Independent Claim 9, for example, is directed to an integrated circuit voltage ramp generator produced using CMOS technology. The integrated circuit voltage ramp generator comprises a capacitance, and a CMOS charging circuit connected to the capacitance. The CMOS charging circuit comprises a current generator having a first resistance, and a circuit connected to the current generator and to the capacitance. The circuit has a second resistance and enables a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance.

Independent Claim 15 is similar to independent Claim 9 except the claim recites that the circuit connected to the current generator is a "degenerate circuit."

Independent Claim 21 is directed to an integrated circuit current ramp generator produced using CMOS technology. The integrated circuit current ramp generator comprises a voltage ramp generator as recited in independent Claim 9, and

a conversion circuit connected to the voltage ramp generator for generating a current ramp. Independent Claim 29 is similar to independent Claim 21 except the claim recites that the circuit connected to the current generator is a "degenerate circuit," and that the conversion circuit is a third resistance.

Independent Claim 36 is a method for generating a ramp voltage, and is similar to independent device Claim 9.

II. The Claims Are Patentable

The Examiner rejected independent Claims 9, 15, 21, 29 and 36 over the Appellants' prior art FIG. 1 in view of the Tanigawa patent and in view of the Lauffenburger patent.

The Appellants' prior art FIG. 1 discloses a ramp generator having a current source **Ig1** with no expressed teaching of the structure thereof, as illustrated in FIG. 1 of the Appellants' specification which is reproduced below. The Examiner cited Tanigawa as disclosing in FIG. 4 a current sink comprising "a current mirror" which has the advantage of gain control, which is also reproduced below.

In re Patent Application of:
GARNIER ET AL.
Serial No. **09/499,060**
Filing Date: **February 4, 2000**
______________________________/

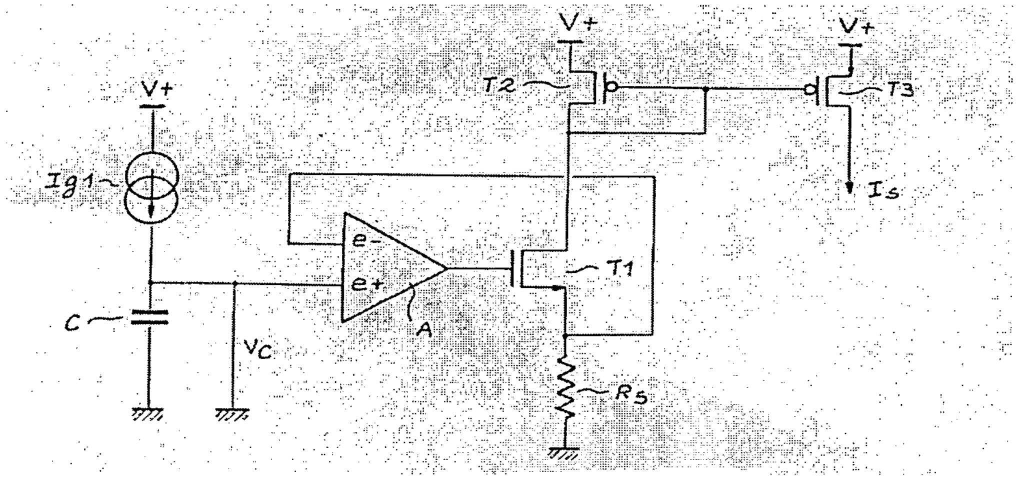

FIG. 1 of Appellants' specification

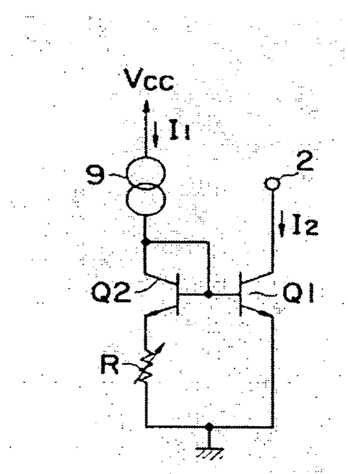

FIG. 4 of Tanigawa

The Examiner has taken the position that it would have been obvious to modify the current sink as disclosed in Tanigawa to a current source, and replace the current source

Ig1 in the Appellants' prior art FIG. 1 with the modified current source for obtaining a constant current with gain control. In addition, the Examiner has taken the position that since this modification yields a circuit identical in structure to the claimed invention, "it must inherently have the same function."

Moreover, the Examiner has further taken the position that it would have been obvious to replace the bipolar transistors in Tanigawa with MOS transistors, and consequently, the current passing through transistor **Q1** of Tanigawa has a square element - just like the current passing through transistor **T5** (FIG. 3 in Appellants' specification) as indicated by the equation on page 6, line 11 of the Appellants' specification.

The Examiner further contends that since a diode-connected MOS transistor has a gate-to-source voltage effectively equal to the threshold voltage thereof, the difference in VGST-Vth <u>must be negligible</u>, as for transistor **T4** discussed on pages 5 and 6 of the Appellants' specification. Thus, regardless of the value of resistance Re, it <u>must also be true that Re x Ig2 >> VGT-Vth</u> (equation on page 6, line 6 of the Appellants' specification) for elements **9** and **Q2** of Tanigawa. Consequently, the Examiner contends that modification of the Appellants' prior art FIG. 1 in view of the Tanigawa patent results in "the capacitance charging current being proportional to a square of a ratio of the second resistance and the first resistance."

The Appellants submit that even if the references were selectively combined as suggested by the Examiner, the

claimed invention is still not produced. In response to the Examiner's position stated above, the Appellants' respectfully submit that it is not necessarily true that Re x Ig2 >> VGST4-Vth4 for elements **9** and **Q2** of Tanigawa. According to the present invention, resistance **Re** is <u>chosen</u> so that Re x Ig2 >> VGST4-Vth4. By selecting the value of the second resistance (i.e., resistance **Re**), this leads to the "capacitance charging current being proportional to a square of a ratio of the second resistance and the first resistance," as in the claimed invention. Calculations supporting selection of resistance **Re** are provided on pages 6 and 7 of the Appellants' specification.

If the value of the second resistance **Re** is not chosen so that this equation is satisfied, then the claim recitation of the "capacitance charging current being proportional to a square of a ratio of the second resistance and the first resistance" is not achieved. Such a choice is not disclosed in Tanigawa. In other words, there is no current specification in Tanigawa, and regardless of the value of the resistance **Re**, it is not necessarily true that Re x Ig2 >> VGST4-Vth4 for elements **9** and **Q2** of Tanigawa.

Still referring to the gain control circuit of the current mirror type as shown in FIG. 4 of Tanigawa, the relationship between the signal current $\mathbf{I_1}$ and the output current $\mathbf{I_2}$ is based upon the equation $\mathbf{I_2 = I_1 * A}$. The Examiner previously characterized the output current $\mathbf{I_2}$ as the capacitance charging current in the present invention. The variable **A** is based upon the equation $\mathbf{exp(V_{BE}/V_T)}$, with $\mathbf{V_T}$ being

a thermal voltage. Referring to column 1, lines 59-61 in Tanigawa, which provides:

> "Therefore, the <u>output current I_2 is set equal to a value A times larger than the input current I_1</u> ..." (Emphasis added.)

Tanigawa thus fails to teach or suggest that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance, as recited in independent Claim 9, for example.

Independent Claim 9 recites that the integrated circuit voltage ramp generator is produced using <u>CMOS technology</u>, and that the charging circuit is a CMOS charging circuit. The CMOS charging circuit includes the first and second resistances, and since these resistances are produced in CMOS technology, their respective spreads can be more readily compensated.

For instance, in CMOS integrated circuits, components typically have broad spreads. With respect to the current ramp generator illustrated in the Appellants' prior art FIG. 1, the spreads of resistors **Rg1** (resistance of the current generator **Ig1**) and **Rs** induce large variations of the gradient **ΔIs/Δt**, as discussed on page 3, lines 5-14 in the background section of the Appellants' specification. As further discussed in the background section of the Appellants' specification, current ramp spreads are adjusted by adjusting the resistance **Rs** with memory points of the fuse type, as discussed on page 3, lines 15-24. This is a tedious and time consuming operation.

The second resistance **Re** in the claimed invention advantageously permits compensation for the variations of the first resistance **Rg1**. The Appellants previously argued that the gain control circuit illustrated in FIG. 4 of Tanigawa is a "conventional gain control circuit of the current mirror type." (column 1, lines 12-13), and is not suitable for semiconductor circuit integration. This argument was made because the Appellants had taken the position that the variable resistance **R** in FIG. 4 of Tanigawa reads on the second resistance **Re** in the claimed invention. Reference is directed to column 1, line 65 through column 2, line 2 in Tanigawa, which provides:

> "However, since the variable resistor **R** is necessary to be connected to the emitter of the transistor **Q2** externally in the circuit shown in FIG. 4, an external leading terminal is required. Accordingly, the circuit of FIG. 4, as it is, is not suitable for semiconductor circuit integration." (Emphasis added.)

In other words, the "second" resistance **R** in Tanigawa is not produced in CMOS technology. This is in sharp contrast to the claimed invention which recites that the voltage ramp generator is produced using CMOS technology, which includes the first and second resistances therein.

The Examiner cited Lauffenburger as disclosing circuitry being integrated onto a single substrate. The Appellants respectfully submit that Lauffenburger fails to provide the deficiencies as noted above, particularly with respect to the capacitance charging current being proportional

to a square of a ratio of the second resistance and the first resistance. In fact, Lauffenburger fails to even mention resistors or resistances with respect to generating a capacitance charging current.

In addition, the Examiner also contends that the discussion pertaining to column 1, line 65 through column 2, line 2 in Tanigawa is discussing a prior art circuit, but "the invention to Tanigawa is using a fixed resistor and a fixed resistor is what is being provided for in the above rejection." The Examiner also references FIGS. 1 and 2 in Tanigawa. Nonetheless, FIGS. 1 and 2 in Tanigawa also fail to teach or suggest that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance. Therefore, even if the references were combined as suggested by the Examiner, the claimed invention is still not produced.

It is also asserted that the prior art references, individually or in combination, do not teach or suggest that 1) the second resistance is chosen so that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance, and that 2) the first and second resistances in the integrated circuit voltage ramp generator are produced using CMOS technology.

Accordingly, it is submitted that independent Claim 9 is patentable over the Appellants' prior art FIG. 1 in view of Tanigawa and Lauffenburger. Independent Claims 15, 21, 29 and 36 are similar to independent Claim 9. In view of the patentability of the independent claims as discussed above, it is submitted that their dependent claims, which recite yet

In re Patent Application of:
GARNIER ET AL.
Serial No. **09/499,060**
Filing Date: **February 4, 2000**
_______________________________/

further distinguishing features, are also patentable over the prior art. Thus, these dependent claims require no further discussion herein.

III. Conclusion

In view of the foregoing arguments, it is submitted that all of the claims are patentable over the prior art. Accordingly, the Board of Patent Appeals and Interferences is respectfully requested to reverse the earlier unfavorable decision of the Examiner.

Respectfully submitted,

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CERTIFICATE OF MAILING

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Susan Jhrawski

In re Patent Application of:
GARNIER ET AL.
Serial No. **09/499,060**
Filing Date: **February 4, 2000**

(9) Appendix

The claims in the appeal are Claims 9-37 and 40 as follows.

9. An integrated circuit voltage ramp generator produced using CMOS technology and comprising:

a capacitance; and

a CMOS charging circuit connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance, said circuit having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance.

10. A voltage ramp generator according to Claim 9, wherein said CMOS charging circuit further comprises a degenerate current mirror circuit.

11. A voltage ramp generator according to Claim 10, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

12. A voltage ramp generator according to Claim 11, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

13. A voltage ramp generator according to Claim 9, wherein said capacitance comprises a gate capacitance of a MOS transistor.

14. A voltage ramp generator according to Claim 9, wherein current generated by said CMOS current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

15. An integrated circuit voltage ramp generator produced using CMOS technology and comprising:

a capacitance; and

a CMOS charging circuit connected to said capacitance and comprising

a current generator having a first resistance, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance.

16. A voltage ramp generator according to Claim 15, wherein said current generator has a first resistance, and said degenerate current mirror circuit has a second resistance such that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

17. A voltage ramp generator according to Claim 15, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS

transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

18. A voltage ramp generator according to Claim 17, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

19. A voltage ramp generator according to Claim 15, wherein said capacitance comprises a gate capacitance of a MOS transistor.

20. A voltage ramp generator according to Claim 15, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

21. An integrated circuit current ramp generator produced using CMOS technology and comprising:

a voltage ramp generator comprising

a capacitance, and

a CMOS charging circuit connected to said capacitance and comprising

a current generator having a first resistance, and

a circuit connected to said current generator and to said capacitance, said circuit having a second resistance and enabling a capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

a conversion circuit connected to said voltage ramp generator for generating a current ramp.

22. A current ramp generator according to Claim 21, wherein said conversion circuit comprises a third resistance.

23. A current ramp generator according to Claim 21, wherein said third resistance comprises an implanted resistance having a positive temperature coefficient.

24. An integrated circuit current ramp generator according to Claim 21, wherein said CMOS charging circuit further comprises a degenerate current mirror circuit.

25. A current ramp generator according to Claim 24, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said current generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a

source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

26. A current ramp generator according to Claim 25, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

27. A current ramp generator according to Claim 21, wherein said capacitance comprises a gate capacitance of a MOS transistor.

28. A current ramp generator according to Claim 21, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

29. An integrated circuit current ramp generator produced using CMOS technology and comprising:

a voltage ramp generator comprising

a capacitance having a first resistance, and

a CMOS charging circuit connected to said capacitance and comprising

a current generator, and

a degenerate current mirror circuit connected to said current generator and to said capacitance, said degenerate current mirror circuit having a second resistance for generating a capacitance charging current that is proportional to a square of a ratio of the second resistance and the first resistance; and

a third resistance connected to said voltage ramp generator for generating a current ramp.

30. A current ramp generator according to Claim 29, wherein said current generator has a first resistance, and said degenerate current mirror circuit has a second resistance such that the capacitance charging current is proportional to a square of a ratio of the second resistance and the first resistance.

31. A current ramp generator according to Claim 29, wherein said third resistance comprises an implanted resistance having a positive temperature coefficient.

32. A current ramp generator according to Claim 29, wherein said degenerate current mirror circuit comprises:

a first MOS transistor having a channel of a first conductivity type comprising a gate, a drain and a source, the drain and the gate being connected to said CMOS current

generator, and the source being connected to said second resistance; and

a second MOS transistor having a channel of the first conductivity type comprising a gate, a drain and a source, the gate being connected to the gate of said first MOS transistor, the source being connected to a supply voltage, and the drain being connected to said capacitance.

33. A current ramp generator according to Claim 32, wherein each of said first and second MOS transistors comprises a P-channel MOS transistor.

34. A current ramp generator according to Claim 29, wherein said capacitance comprises a gate capacitance of a MOS transistor.

35. A current ramp generator according to Claim 29, wherein current generated by said current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.

In re Patent Application of:
GARNIER ET AL.
Serial No. **09/499,060**
Filing Date: **February 4, 2000**

36. A method for generating a ramp voltage comprising:

generating a capacitance charging current using an integrated circuit charging circuit produced using CMOS technology and comprising a current generator having a first resistance and a circuit connected to the generator, the circuit having a second resistance and enabling the capacitance charging current to be proportional to a square of a ratio of the second resistance and the first resistance; and

charging a capacitance with the capacitance charging current for generating the ramp voltage.

37. A method according to Claim 36, wherein the circuit further comprises a degenerate current mirror circuit.

40. A method according to Claim 36, wherein current generated by the current generator is based upon the equation:

$$Ig2 = K2 \times \frac{Vg2}{Rg2}$$

where Ig2 is the current, K2 is a proportionality coefficient, Rg2 is the first resistance, and Vg2 is a reference voltage proportional to the quantity $k\frac{T}{q}$, where k is the Boltzmann constant, T is absolute temperature, and q is the charge of an electron.